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EXAMINER	
THAI, LUAN C	
ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,256	BLACKSHEAR ET AL.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-14 and 21-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office action is responsive to the amendment filed February 26, 2003.

Claims **1-14** and newly added claims **21-26** are pending in this application.

Claims **15-20** have been canceled.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features of *a thermal material* between a top of the memory chip package and a bottom of an adjacent substrate, as recited in claims 6, 13, and 26; and the features of *the space between a top of the memory chip package and a bottom of the adjacent substrate* being *greater than a height of the memory chip package,* as recited in claim 21; must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Newly added claims **21-26** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification, as originally filed, does not disclose that a space, which is formed between a top of the memory chip package and a bottom of the adjacent

substrate by substrate spacers, is greater than a height of the memory chip package, as recited in claim 21.

Claims **22-26** are rejected since each includes the limitations of independent claim **21**.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Newly added claims **21-26** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In newly added claim **21**, the recitations of "a gap between a top of said memory chip package and a bottom of an adjacent substrate" and of "a space between a top of said memory chip package and a bottom of an adjacent substrate" are unclear as to whether these limitation imply two similar or two different limitations.

Claims **22-26** are rejected since each includes the limitations of independent claim **21**.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 1, 3, and 7, are rejected under 35 U.S.C. 102(e) as being anticipated by Nakajima (US 2002/0086459).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1 and 3, Nakajima discloses (see specifically figures 2B and 4) a memory structure comprising: a plurality of adjacent substrates (10c) stacked one on another and electrically connected to one another via a plurality of connectors (23/25); a single memory chip package (11) (see figure 4, paragraph [0035]) mounted on each of substrates (10c); a plurality of package spacers (33b) (e.g., solder balls 33b) connecting the memory chip package (11) with the substrate (10c). It appears from Nakajima's figure 2B that the connectors (25) have the heights higher than the height from the surface of substrate on which the chip package (11) is mounted to the top of the chip package (11); thus, the connectors (23/25) have a size sufficient to form a space between two adjacent substrates (10c) and a space (or a gap) between the top surface of the chip package (11) and the bottom of the adjacent substrate (10c), and wherein the space is larger than a height of the memory chip packages (11). Nakajima further discloses the memory chip packages (11) and the substrates (10c) include identical electrical connections (23/25).

Regarding claim 7, although Nakajima does not explicitly disclose the memory chip package having an array of memory elements, this feature is taken to be inherent in Nakajima's device since Nakajima's chip package (11) appears to be a memory chip package and a memory chip package would have to contain an array of memory elements. Note that US Pat. 5,694,366 to Chevallier et al., Col. 1, lines 48+, is cited to support the inherency position above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4-6, 8, 10-14, 21, and 23-26, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 2002/0086459) in view of Miremadi et al (5,854,507 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 8, 10, 14, 21,23, and 25, Nakajima discloses all the limitations of the claimed invention as detailed above except for the memory chip package including a single memory chip.

A memory chip package comprising a single memory chip is conventionally used in the art, especially in semiconductor memory device art, as taught by Miremadi et al. who disclose (see specifically figure 2) a memory chip package (21) comprising a substrate (25) and a single memory chip 23 mounted thereon. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a single memory chip package, as taught by Miremadi et al., in Nakajima memory chip package structure, in order to simplify the process of forming the memory chip package.

Regarding claims 5 and 12, Nakajima discloses all the limitations of the claimed invention as detailed above except for the connectors comprising solder balls.

Miremadi et al. while related to a similar memory structure design teach (see specifically figures 7-8) the connectors (19), which make electrical connections between two adjacent substrates (51-57), comprising solder balls (19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply Miremadi et al's teachings to Nakajima memory structure by using solder balls for constructing electrical connections between two substrates, since solder balls are conventional in the art for making electrical connections between two substrates, as taught by Miremadi et al.

Regarding claims 4, 11 and 24, Nakajima discloses all the limitations of the claimed invention as detailed above except for teaching plurality of memory chip packages mounted on each substrate.

Miremadi et al. while related to a similar memory structure design teach the memory structure can feature multiple memory chip packages on each substrate (Col. 4, lines 35+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miremadi et al.'s memory chip structure by mounting multiple memory chip packages on each substrate, as taught by Miremadi et al, in order to make the memory structure being larger in capacity.

Regarding claims 6, 13, and 26, Nakajima discloses all the limitations of the claimed invention as detailed above except for a thermal material between a top of the chip package and a bottom of an adjacent substrate.

Miremadi et al. while related to a similar memory structure design teach (see specifically figures 7-8) a thermal material (38) between a top of the chip package (25/65) and a bottom (61) of an adjacent substrate (51) in order to improve the heat

dissipating for the memory chip packages (Col. 8, lines 43+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a thermal material between a top of the chip package and a bottom of an adjacent substrate, as taught by Miremadi et al, to Nakajima memory structure in order to improve the heat dissipating for the memory chip packages.

10. Claims 2, 9, and 22, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima (US 2002/0086459) and Miremadi et al (5,854,507 of record), as applied to claims 1, 8, and 21 above, and in further in view of Moresco et al. (5,655,290 of record).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 2, 9, and 22, the proposed memory structure of Nakajima and Miremadi et al discloses all the limitations of the claimed invention as detailed above except for the process step of testing the memory chip package before mounting the package on the substrates. Noted, "Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is obvious from a product of the prior art, the claim is unpatentable ". In re Thorpe, 227 U.S.P.Q. 964 (Fed. Cir. 1985). (MPEP 2113).

Claims 2, 9, and 22 are product-by-process claims depending from claims 1, 8 and 21, respectively. The product recited by claims 2, 9, and 22 are identical to the product

recited by claims 1, 8 and 21, and as claims 1, 8 and 21 are rejected as being obvious over the prior art, claims 2, 9, and 22 are also rejected.

Moreover, testing a semiconductor chip or a chip package before mounting on a substrate is a standard procedure in semiconductor art, as taught by Moresco et al. (Col. 4, lines 1+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to test the memory chip package in the proposed memory structure of Nakajima and Miremadi et al in order to select only the good chip package to be mounted on the substrate.

Conclusion

11. Applicant's arguments with respect to claims **1-14** and newly added claims **21-26** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the changes (the underlined portions) in claims 1, 6, 8, and13, and newly added claims 21-26 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
June 18, 2003

DAVID L. TALBOTT
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